TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention

STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SIGE AND/OR Si:C

Application Number:

Date:

First Named Applicant:

Huilong Zhu

Confirmation Number:

Attorney Docket Number: FIS920030375

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Documents being submitted:	Files	
us-request	FIS920030375US1-usrequ.xml	
	us-request.dtd	
	us-request.xsl	
us-assignment	FIS920030375US1-usassn.xml	
	us-assignment.xsl	
	us-assignment.dtd	
	FIS920030375assign1.tif	
	FIS920030375assign2.tif	
us-fee-sheet	FIS920030375US1-usfees.xml	
	us-fee-sheet.xsl	
	us-fee-sheet.dtd	
us-declaration	FIS920030375dec1.tif	
us-declaration	FIS920030375dec2.tif	
application-body	FIS920030375US1-trans.xml	
	us-application-body.xsl	
	application-body.dtd	
	wipo.ent	
	mathml2.dtd	
	mathml2-qname-1.mod	
	isoamsa.ent	
	isoamsb.ent	
	isoamsc.ent	
	isoamsn.ent	
	isoamso.ent	
	isoamsr.ent	
	isogrk3.ent	
	isomfrk.ent	
	isomopf.ent	
	isomscr.ent	
	isotech.ent	
	isobox.ent	
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	isocyr2.ent	
	isodia.ent	
	isolat1.ent	
	isolat2.ent	
	isonum.ent	
	isopub.ent	
	mmlextra.ent	
	mmlalias.ent	
	soextblx.dtd	
	FIS920030375sheet1.tif	
	FIS920030375sheet2.tif	
	FIS920030375sheet3.tif	
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	FIS920030375sheet5.tif	
	FIS920030375sheet6.tif	
	FIS920030375sheet7.tif	
	FIS920030375sheet8.tif	

FIS920030375sheet9.tif
Comments
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